WHAT IS CLAIMED IS:

1. A method for performing a rounding step of a floating point computation on at least one floating point operand to preserve an inexact status, the method comprising:

receiving the at least one operand and determining whether the at least one operand is inexact;

determining whether an intermediate result of a floating point computation is inexact; and

rounding the intermediate result based on whether the at least one operand is inexact and whether the intermediate result is inexact to preserve an inexact status of the at least one operand and the intermediate result.

2. The method of claim 1, wherein determining whether the at least one operand is inexact comprises analyzing embedded information within the at least one operand.

3. The method of claim 1, wherein determining whether the at least one operand is inexact comprises analyzing information stored in a register.

4. The method of claim 1, wherein determining whether the intermediate result is inexact comprises analyzing at least one digit of the intermediate result.

5. The method of claim 4, wherein determining whether the intermediate result is inexact comprises analyzing a least significant digit of the intermediate result, a guard digit, and a sticky digit.

6. The method of claim 1, wherein rounding the intermediate result comprises:

altering a least significant digit of the intermediate result if either the at least one operand is inexact or the intermediate result is inexact; and

altering a second least significant digit of the intermediate result if the second least significant digit of the intermediate result is equivalent to a specified value and either the at least one operand is inexact or the intermediate result is inexact.

7. The method of claim 6, wherein the specified value is a binary one.

8. The method of claim 1, further comprising receiving a rounding mode selection signal.

9. The method of claim 8, wherein the step of rounding further comprises rounding the intermediate result to preserve the inexact status if the rounding mode selection signal indicates a rounding mode to preserve inexact status.

10. A computer-readable medium on which is stored a set of instructions for performing a rounding step of a floating point computation on at least one floating

point operand to preserve an inexact status, which when executed performs steps comprising:

determining whether the at least one operand is inexact;

determining whether the intermediate result of a floating point computation is inexact; and

rounding the intermediate result based on whether the at least one operand is inexact and whether the intermediate result is inexact to preserve an inexact status of the at least one operand and the intermediate result.

11. The computer-readable medium of claim 10, wherein determining whether the at least one operand is inexact comprises analyzing embedded information within the at least one operand.

12. The computer-readable medium of claim 10, wherein determining whether the at least one operand is inexact comprises analyzing information stored in a register.

13. The computer-readable medium of claim 10, wherein determining whether the intermediate result is inexact comprises analyzing at least one digit of the intermediate result.

14. The computer-readable medium of claim 13, wherein determining whether the intermediate result is inexact comprises analyzing a least significant digit of the intermediate result, a guard digit, and a sticky digit.

15. The computer-readable medium of claim 10, wherein rounding the intermediate result comprises:

altering a least significant digit of the intermediate result if either the at least one operand is inexact or the intermediate result is inexact; and

altering a second least significant digit of the intermediate result if the second least significant digit of the intermediate result is equivalent to a specified value and either the at least one operand is inexact or the intermediate result is inexact.

16. The computer-readable medium of claim 15, wherein the specified value is a binary one.

17. The computer-readable medium of claim 10, wherein the step of rounding further comprises rounding the intermediate result to preserve the inexact status if a rounding mode selection signal indicates a rounding mode to preserve inexact status.

18. A system for performing a rounding step of a floating point computation on at least one floating point operand to preserve an inexact status, the system comprising:

a functional core unit for generating an intermediate result based on the at least one operand; and

a first rounding unit configured to receive the intermediate result and round the intermediate result based on whether the at least one operand is inexact and whether the intermediate result is inexact to preserve the inexact status of the at least one operand and the intermediate result.

19. The system of claim 18, wherein the first rounding unit is configured to:

alter a least significant digit of the intermediate result if either the at least one operand is inexact or the intermediate result is inexact; and

alter a second least significant digit of the intermediate result if the second least significant digit of the intermediate result is equivalent to a specified value and either the at least one operand is inexact or the intermediate result is inexact.

20. The system of claim 19, wherein the specified value is a binary one.

21. The system of claim 18, further comprising:

at least one other rounding unit for rounding the intermediate result; and

a multiplexer for selecting either the rounded intermediate result from the first rounding unit or the at least one other rounding unit based on a rounding mode selection signal.

22. A system for performing a rounding step of a floating point computation on at least one floating point operand to preserve an inexact status, the system comprising:

first determining means for determining whether the at least one operand is inexact;

second determining means for determining whether an intermediate result of a floating point computation is inexact; and

rounding means for rounding the intermediate result based on whether the at least one operand is inexact and whether the intermediate result is inexact to preserve an inexact status of the at least one operand and the intermediate result.

23. The system of claim 12, wherein first determining means analyzes embedded information within the at least one operand.

24. The system of claim 22, wherein first determining means analyzes information stored in a register.

25. The system of claim 22, wherein second determining means analyzes at least one ~~bit~~ digit of the intermediate result.

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26. The system of claim 25, wherein second determining means analyzes a least significant digit of the intermediate result, a guard digit, and a sticky digit.

27. The system of claim 22, wherein rounding means alters a least significant digit of the intermediate result if either the at least one operand is inexact or the intermediate result is inexact and alters a second least significant digit of the intermediate result if the second least significant digit of the intermediate result is equivalent to a specified value and either the at least one operand is inexact or the intermediate result is inexact.

28. The system of claim 22, further comprising receiving means for receiving a rounding mode selection signal.

29. The system of claim 28, wherein the rounding means rounds the intermediate result to preserve the inexact status if the rounding mode selection signal indicates a rounding mode to preserve inexact status.